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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,534	08/05/2003	Yoshihiro Sugita	030862	6460

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,534	SUGITA ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 14, 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Nallan et al. (US/2004/0002223).

Re claim 8, Nallan et al. disclose a method manufacturing of a semiconductor device comprising sequential steps of: forming an insulating film (402) made of ZrO_2 or HfO_2 over a surface of a semiconductor substrate (414); covering a partial surface area of the insulating film with a mask pattern (406) (i.e., gate pattern); exposing a region of the insulating film (402) not covered with the mask pattern to one plasma selected from a group consisting of nitrogen plasma, argon plasma and ammonia plasma (see Page 1, Paragraph 0016); following the step of exposing region of the insulating film not covered with the mask pattern to on plasma selected

form the group consisting of nitrogen plasma, argon plasma and ammonia plasma and etching a portion of the insulating film by using the mask pattern as a mask (see Page 1, Paragraph 0016; Page 2, Paragraph 0026 – 0027; Pages 3 – 4; Figs. 4a and 4b) .

Re claim 11, Nallan et al. disclose a method manufacturing of a semiconductor device comprising sequential steps of: forming an insulating film (402) made of zirconia or hafnia over a surface of a semiconductor substrate (414); forming a gate electrode (406) on a partial surface area of the insulating film (402); exposing a region of the insulating film not covered with the gate electrode to one plasma selected from a group consisting of nitrogen plasma, argon plasma and ammonia plasma (see Page 1, Paragraph 0016); following the step of exposing region of the insulating film not covered with the mask pattern to on plasma selected form the group consisting of nitrogen plasma, argon plasma and ammonia plasma and etching a portion of the insulating film by using the gate electrode pattern as mask (see Page 1, Paragraph 0016; Page 2, Paragraph 0026 – 0027; Pages 3 – 4; Figs. 4a and 4b) .

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nallan et al. (US/2004/0002223), as applied in Paragraph 3 above, and in view of Tsunashima et al. (US/2001/0023120).

Re claim 9 as applied to claim 8 in Paragraph 3 above, Nallan et al. disclose all the claimed limitations including removing the gate dielectric layer.

However, Nallan et al. do not specifically disclose using sulfuric acid or mixture liquid of sulfuric acid and hydrogen peroxide to etch the insulating layer.

Tsunashima et al. disclose using the sulfuric acid in order to remove the insulating layer comprises zirconium oxide layer (see Page 8, Paragraph 00140).

Both Nallan et al. and Tsunashima et al. teachings are directed to fabricating MOSFET device including forming of the high K gate dielectric layer. Therefore, the teachings of Nallan et al. and Tsunashima et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Nallan et al. reference with etching of the insulating layer using sulfuric acid as taught by Tsunashima et al. in order to form a patterned gate stack by using sulfuric acid to remove (etch) the amorphous metal oxide layer insulating (gate dielectric film).

6. Claims 1-3, 7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama (US/6,150,221) in view of Callegari et al. (US/6,573,197).

Re claim 1, Aoyama discloses a method of manufacturing semiconductor device the method comprises: forming an a gate insulating film (2) (see Fig. 4A) over a surface of a semiconductor substrate (1); covering a partial surface area of the insulating film with a mask (i.e., gate electrode) pattern (3); implanting ions into a region of the insulating film (2) not covered with the mask pattern (3) (see Fig. 4B) using the gate pattern as a mask to give damages to the insulating film to transform the region of the insulating film and the substrate not covered by the gate electrode in to amorphous (i.e., the ion implant such as Si, Ge or As used is capable of to amorphize the gate insulating layer as well as the substrate); following the step of implanting ions into a region of the insulating film not covered with the mask pattern to transform the region of the insulating film to an amorphous state, and etching a portion of the insulating film by using the mask pattern as a mask, (see Fig. 4C) (see Figs. 4A-4D; Col. 4, line 21 – Col 5, line 5).

Although it is well known in the art to use high dielectric constant gate insulating material such as ZrO_2 or HfO_2, Aoyama does not specifically disclose the insulating film (i.e., the gate dielectric film) being zirconia (ZrO_2) or hafnia (HfO_2).

Callegari et al. disclose a method fabricating FET device having high dielectric constant gate insulating layer (see Abstract). As Callegari et al. disclose that "A variety of high-dielectric constant, i.e., high-k, materials such as binary metal oxides including aluminum oxide (Al_2O_3), **zirconium oxide (ZrO_2), hafnium oxide (HfO_2),** lanthanum oxide (La_2O_3), titanium oxide (TiO_2), as well as their silicates and aluminates; and perovskite-type oxides including a titanate system material such as barium titanate, strontium titanate, barium strontium titanate (BST), lead titanate, lead zirconate titanate, lead lanthanum zirconate titanate, barium lanthanum

titanate, barium zirconium titanate; a niobate or tantalate system material such as lead magnesium niobate, lithium niobate, lithium tantalate, potassium niobate, strontium aluminum tantalate and potassium tantalum niobate; a tungsten-bronze system material such as barium strontium niobate, lead barium niobate, barium titanium niobate; and Bi-layered perovskite system material such as strontium bismuth tantalate, bismuth titanate are known in the art." (see Callegari et al. Col. 1, lines 35-52).

Both Aoyama and Callegari et al. teachings are directed to fabricating MOSFET device including forming of the gate dielectric layer. Therefore, the teachings of Aoyama and Callegari et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Aoyama reference with the gate insulating film comprises zirconia or hafnia as taught by Callegari et al. because the high K dielectric layer such as ZrO_2 or HfO_2 exhibit high thermal stability and low leakage current and as result the device performance would have been enhanced as well known in the art.

Re claim 2, as applied to claim 1 above, Aoyama and Callegari et al. in combination disclose all the claimed limitations including the limitations during implanting ions into a region of the insulating film (2) not covered with the mask pattern, the ions being ions of an element not generating carriers when the ions are implanted into the semiconductor substrate (see Figs. 4A-4D; Col. 4, line 21 – Col 5, line 5; Callegari et al. Col. 1, lines 35-52).

Re claim 3, as applied to claim 1 above, Aoyama and Callegari et al. in combination disclose all the claimed limitations including the limitations the ions being ions of an element

selected from a group consisting of silicon, germanium, argon and xenon (see Figs. 4A-4D; Col. 4, line 21 – Col 5, line 5; Callegari et al. Col. 1, lines 35-52).

Re claim 7, Aoyama discloses a method manufacturing of a semiconductor device comprising steps of: forming a gate insulating film (2) over a surface of a semiconductor substrate (1); covering a partial surface area of the insulating film with a mask pattern; transforming a region of the insulating film not covered with the mask pattern to an amorphous state and following the step of transforming a region of the insulating film to an amorphous state etching the insulating film transformed to the amorphous state by using the mask pattern as a mask (see Figs. 4A-4D; Col. 4, line 21 – Col 5, line 5).

Although it is well known in the art to use high dielectric constant gate insulating material such as ZrO_2 or HfO_2, Aoyama does not specifically disclose the insulating film (i.e., the gate dielectric film) being zirconia (ZrO_2) or hafnia (HfO_2).

Callegari et al. disclose a method fabricating FET device having high dielectric constant gate insulating layer (see Abstract). As Callegari et al. disclose that "A variety of high-dielectric constant, i.e., high-k, materials such as binary metal oxides including aluminum oxide (Al_2O_3), **zirconium oxide (ZrO_2), hafnium oxide (HfO_2),** lanthanum oxide (La_2O_3), titanium oxide (TiO_2), as well as their silicates and aluminates; and perovskite-type oxides including a titanate system material such as barium titanate, strontium titanate, barium strontium titanate (BST), lead titanate, lead zirconate titanate, lead lanthanum zirconate titanate, barium lanthanum titanate, barium zirconium titanate; a niobate or tantalate system material such as lead magnesium niobate, lithium niobate, lithium tantalate, potassium niobate, strontium aluminum tantalate and potassium tantalum niobate; a tungsten-bronze system material such as barium

strontium niobate, lead barium niobate, barium titanium niobate; and Bi-layered perovskite system material such as strontium bismuth tantalate, bismuth titanate are known in the art." (See Callegari et al. Col. 1, lines 35-52).

Both Aoyama and Callegari et al. teachings are directed to fabricating MOSFET device including forming of the gate dielectric layer. Therefore, the teachings of Aoyama and Callegari et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Aoyama reference with the gate insulating film comprises zirconia or hafnia as taught by Callegari et al. because the high K dielectric layer such as ZrO_2 or HfO_2 exhibit high thermal stability and low leakage current and as result the device performance would have been enhanced as well known in the art.

Re claim 10, Aoyama discloses a method manufacturing of a semiconductor device comprising steps of: forming an insulating film (2) over a surface of a semiconductor substrate (1); forming a gate electrode (3) on a partial surface area of the insulating film (2); implanting ions into a region of the insulating film (2) not covered with the gate electrode to transform the region of the insulating film and the substrate not covered by the gate electrode in to amorphous (i.e., the ion implant such as Si, Ge or As used is capable of to amorphize the gate insulating layer as well as the substrate); etching a portion of the gate insulating film; implanting impurity ions (7 8) into a surface layer of the semiconductor substrate (1) on both sides of the gate electrode (3); implanting impurity ions into a surface layer of the semiconductor substrate on both sides of the gate electrode (3) using the gate electrode as a mask (see Figs. 4A-4D; Col. 4, line 21 – Col 5, line 5).

Although it is well known in the art to use high dielectric constant gate insulating material such as ZrO_2 or HfO_2, Aoyama does not specifically disclose the insulating film (i.e., the gate dielectric film) being zirconia (ZrO_2) or hafnia (HfO_2).

Callegari et al. disclose a method fabricating FET device having high dielectric constant gate insulating layer (see Abstract). As Callegari et al. disclose that "A variety of high-dielectric constant, i.e., high-k, materials such as binary metal oxides including aluminum oxide (Al_2O_3), **zirconium oxide (ZrO_2), hafnium oxide (HfO_2),** lanthanum oxide (La_2O_3), titanium oxide (TiO_2), as well as their silicates and aluminates; and perovskite-type oxides including a titanate system material such as barium titanate, strontium titanate, barium strontium titanate (BST), lead titanate, lead zirconate titanate, lead lanthanum zirconate titanate, barium lanthanum titanate, barium zirconium titanate; a niobate or tantalate system material such as lead magnesium niobate, lithium niobate, lithium tantalate, potassium niobate, strontium aluminum tantalate and potassium tantalum niobate; a tungsten-bronze system material such as barium strontium niobate, lead barium niobate, barium titanium niobate; and Bi-layered perovskite system material such as strontium bismuth tantalate, bismuth titanate are known in the art." (See Callegari et al. Col. 1, lines 35-52).

Both Aoyama and Callegari et al. teachings are directed to fabricating MOSFET device including forming of the gate dielectric layer. Therefore, the teachings of Aoyama and Callegari et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Aoyama reference with the gate insulating film comprises zirconia or hafnia as taught by Callegari et al. because the high K

dielectric layer such as ZrO_2 or HfO_2 exhibit high thermal stability and low leakage current and as result the device performance would have been enhanced as well known in the art.

7. Claims 4-6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama (US/6,150,221) in view of Callegari et al. (US/6,573,197), and further in view of Tsunashima et al. (US/2001/0023120).

Re claims 4, 5, and 6, as applied to claims 1-3 respectively in Paragraph 5 above, Aoyama and Callegari et al. in combination disclose all the claimed limitations including removing the gate dielectric layer.

However, the combination of Aoyama and Callegari et al. do not specifically disclose using sulfuric acid or mixture liquid of sulfuric acid and hydrogen peroxide to etch the insulating layer.

Tsunashima et al. disclose using the sulfuric acid in order to remove the insulating layer comprises zirconium oxide layer (see Page 8, Paragraph 00140).

Aoyama, Callegari et al., and Tsunashima et al. teachings are directed to fabricating MOSFET device including forming of the gate dielectric layer. Therefore, the teachings of Aoyama, Callegari et al., and Tsunashima et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Aoyama and Callegari et al. reference with etching of the insulating layer using sulfuric acid as taught by Tsunashima et al. in order to form patterned gate stack by using sulfuric acid to remove (etch) the amorphous metal oxide layer insulating (gate dielectric film).

Re claim 12, Aoyama discloses a method of manufacturing semiconductor device the method comprises: forming an a gate insulating film (2) (see Fig. 4A) over a surface of a semiconductor substrate (1); covering a partial surface area of the insulating film with a mask (i.e., gate electrode) pattern (3); implanting ions into a region of the insulating film (2) not covered with the mask pattern (3) (see Fig. 4B) using the gate pattern as a mask to transform the region of the insulating film not covered with the mask pattern to amorphous state and following the implanting ions into a region of the sinsulating film not covered with the mask pattern to transform the region to an amorphous state (i.e., the ion implant such as Si, Ge or As used is capable of to amorphize the gate insulating layer as well as the substrate) , etching a portion of the insulating film by using the mask pattern as a mask (see Fig. 4C) (see Figs. 4A-4D; Col. 4, line 21 – Col 5, line 5).

Although it is well known in the art to use high dielectric constant gate insulating material such as ZrO_2 or HfO_2, Aoyama does not specifically disclose the insulating film (i.e., the gate dielectric film) being zirconia (ZrO_2) or hafnia (HfO_2).

Callegari et al. disclose a method fabricating FET device having high dielectric constant gate insulating layer (see Abstract). As Callegari et al. disclose that "A variety of high-dielectric constant, i.e., high-k, materials such as binary metal oxides including aluminum oxide (Al_2O_3), **zirconium oxide (ZrO_2), hafnium oxide (HfO_2),** lanthanum oxide (La_2O_3), titanium oxide (TiO_2), as well as their silicates and aluminates; and perovskite-type oxides including a titanate system material such as barium titanate, strontium titanate, barium strontium titanate (BST), lead titanate, lead zirconate titanate, lead lanthanum zirconate titanate, barium lanthanum titanate, barium zirconium titanate; a niobate or tantalate system material such as lead

magnesium niobate, lithium niobate, lithium tantalate, potassium niobate, strontium aluminum tantalate and potassium tantalum niobate; a tungsten-bronze system material such as barium strontium niobate, lead barium niobate, barium titanium niobate; and Bi-layered perovskite system material such as strontium bismuth tantalate, bismuth titanate are known in the art." (see Callegari et al. Col. 1, lines 35-52).

Both Aoyama and Callegari et al. teachings are directed to fabricating MOSFET device including forming of the gate dielectric layer. Therefore, the teachings of Aoyama and Callegari et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Aoyama reference with the gate insulating film comprises zirconia or hafnia as taught by Callegari et al. because the high K dielectric layer such as ZrO_2 or HfO_2 exhibit high thermal stability and low leakage current and as result the device performance would have been enhanced as well known in the art.

However, the combination of Aoyama and Callegari et al. do not specifically disclose using sulfuric acid or mixture liquid of sulfuric acid and hydrogen peroxide to etch the insulating layer.

Tsunashima et al. disclose using the sulfuric acid in order to remove the insulating layer comprises zirconium oxide layer (see Page 8, Paragraph 00140).

Aoyama, Callegari et al., and Tsunashima et al. teachings are directed to fabricating MOSFET device including forming of the gate dielectric layer. Therefore, the teachings of Aoyama, Callegari et al., and Tsunashima et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Aoyama and Callegari et al. reference with etching of the insulating layer using sulfuric acid as taught by Tsunashima et al. in order to form patterned gate stack by using sulfuric acid to remove (etch) the amorphous metal oxide layer insulating (gate dielectric film).

Response to Arguments

8. Applicants' arguments filed on March 29, 2005 have been fully considered but they are not persuasive.

With respect to claims 8 and 11, Applicants argue that "the region of the film exposed to plasma (N, AR or NH_3) is etched *after* the plasma treatment "

In response to applicants' argument, it is respectfully submitted that Nallan et al., as applied in Paragraph 3 above, teach all the claimed limitations including exposing of the substrate to the plasma treatment then etching of the gate dielectric layer 402 after the plasma treatment. (See Figs. 4a and 4b).

Claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the rejection of claims 8 and 11 under 35 U.S.C. 102 is deemed proper.

With respect to claims rejections of claims 1-7, 9, and 10, applicants arguments pertaining to U.S. Patent 5,468,657 and IEEE references are moot because these references

neither part of the prior art applied in the rejections nor recited by the Office as pertinent art and have no relevant fact to the issue in hand.

With respect to 1-3, 7 and 10, the combination of Aoyama '221 and Callegari et al. disclose the claimed invention of the instant application. Therefore, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Similarly the combination of Aoyama '221, Callegari et al. and Tsunashima et al. '002310 also teach all the claimed limitations as applied to in Paragraph 6 herein above.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

9. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Examiner
Art Unit 2823

BK
May 15, 2005